OPTIMIZATION OF PAPER SUBSTRATES FOR APPLICATION IN PAPER-BASED FETS

D. Gaspar, L. Pereira, E. Fortunato and R. Martins

MEON, dfpgaspar@gmail.com; lmnp@fct.unl.pt; emf@fct.unl.pt; rm@uninova.pt

www.cenimat.fct.unl.pt

Abstract

Nowadays paper substrates are considered as a potential "electronic" material with growing interest among scientific community, due to the possibility of having low cost, disposable and recyclable electric devices. Many research groups have being working on the optimization of cellulose based substrates for electronic applications either by using paper as a support for devices, as dielectric layer in field effect transistors (FETs) or by functionalizing it with conductor/semiconductor materials. In this work we present insights on cellulose-based substrates and device's configuration aiming the application in electronic devices, such as FETs.

Dual-gate (in-plane) transistors using gallium indium zinc oxide (GIZO) (1:2:2 mol%) deposited by rf-magnetron sputtering as semiconductor, were produced on the surface of a paper substrate. Using this configuration we are able to tune the on-voltage from -20.5 to 5.5 V by changing the voltage at the secondary gate from +15 V to -15 V.

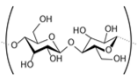
Concerning the paper's tailoring, it was observed that the gate leakage current and susceptibility to the relative humidity in paper FETs can be reduced using a dense micro/nano fiber cellulose (M-NFC) paper as dielectric. Moreover, it was shown that the addition of HCl to M-NFC pulp can improve the FETs' performance, achieving saturation mobility up to 16 $cm^2 V^{-1} s^{-1}$, with an I_{ON}/I_{OFF} ratio close to 10^5.

Paper as dielectric

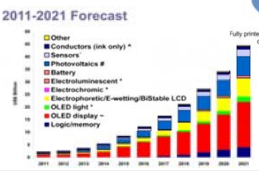
Why electronic on/with paper?

Flexible, lightweight, cheapest and ecofriendly electronic

- Most abundant biopolymer , recyclable and environmentally friendly
- Flexible and unbreakable
- Low cost material (500x less than PET)
- Established production technology (100 km/h)
- Good dielectric properties
- Recyclable



Impact



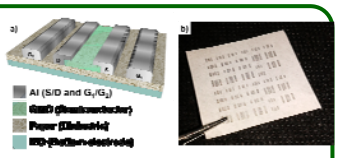
Challenges

- Rough and porous surface
- Electric properties suitable to be used as dielectric

Devices engineering

➢ Dual gate (DG) planar design

- Symmetric/asymmetric voltage can be applied in two gate electrodes.
- V_{On}, threshold voltage (V_{th}) and operation mode modulation through secondary gate electrode:
  → advantageous for logic applications.
- Reported dual-gate FETs involve complex fabrication processes.



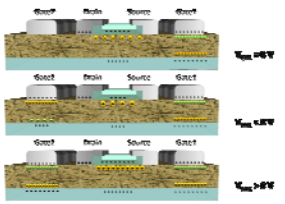
a) Schematic of the dual-gate GIZO paper FETs structure using the paper as the dielectric gate and b) DGFETs produced on paper.

➢ Process:

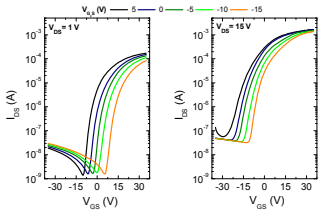
- Easy (shadow masks) and low-temperature process.
- Dielectric layer unnecessary → paper as dielectric!

DG-FETs Characteristics

- Semiconductor – 40 nm of GIZO (1:2:2 mol%) deposited by rf-magnetron sputtering
- Source/Drain (S/D)) and Gate (1 and 2) – 150 nm of Al by e-beam evaporation
- Back electrode - 200 nm thick IZO (In_2O_3-ZnO; 89.3:10.7 wt.%) by rf-magnetron sputtering
- Semiconductor, S/D and G1/2 were patterned by shadow mask, with width-to-length ratio (W/L) of 6.1.



Schematic representation of the operation mode of the paper DGFETs in function of the VGS2.



I_{DS}-V_{GS} transfer characteristics of the paper gated GIZO FETs at V_{DS}=1 and 15V.

Comparison of electrical parameters of the paper based DGFETs for different G2 bias (V_{DS} = 15 V).

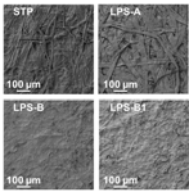
V_{GS2} (V)	I_{ON}/I_{OFF}	V_{ON} (V)	S (V dec^{-1})	μ_{SAT} ($cm^{-2} V^{-1} s^{-1}$)
-15	$4.34x10^4$	-12.5	2.27	2.96
-10	$4.08x10^4$	-18	2.67	2.52
-5	$3.98x10^4$	-21.5	2.90	2.60
0	$3.98x10^4$	-25	3.42	3.04
5	$2.87x10^4$	-30	3.91	2.74

- A negative V_{GS2} partially depletes the accumulation channel. To compensate the depletion, the first gate bias has to be adjusted, which makes the V_{ON} move toward positive direction.
- Positive V_{GS2} makes the channel more conducting. This creates an additional current that effectively shifts the V_{ON} toward negative voltage.
- In saturation V_{DS} is high and screens the effect of V_{GS2}, the V_{ON} variation is lower than in linear regime.

Paper engineering

➢ Paper samples

- STP – Standard tracing paper: Commercial paper
- LPS-A – Long fibbers paper
  - Bleached Softwood Kraft Pulp (BSKP)
- LPS-B – Small fibbers paper, micro-nano fibril cellulose (M-NFC)
  - LPS-B – Pure M-NFC paper
  - LPS-B1 – M-NFC paper with extra anionic charge (HCl)



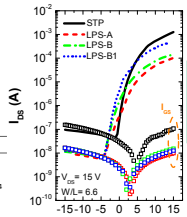
	STP	LPS-A	LPS-B	LPS-B1
C (µF.cm^{-2})	1.7	1.8	0.24	0.05
ρ (Ω.cm)	$4.9x10^7$	$4.3x10^8$	$1.4x10^9$	$1.3x10^9$

FETs Characteristics

- Semiconductor – 40 nm of GIZO (1:2:2 mol%) deposited by rf-magnetron sputtering
- Source/Drain (S/D)) – 150 nm of Al by e-beam evaporation
- Gate - 200 nm thick IZO (In_2O_3-ZnO; 89.3:10.7 wt.%) by rf-magnetron sputtering.

	STP	LPS-A	LPS-B	LPS-B1
μ_{SAT} ($cm^{-2} V^{-1} s^{-1}$)	2.3	0.14	0.94	16
V_{ON} (V)	-2.5	-5.5	-4.7	-4.8
I_{ON}/I_{OFF}	$2.5x10^4$	$1.7x10^4$	$2.2x10^4$	$7.5x10^4$
S (V dec^{-1})	0.89	2.1	1.6	1.3

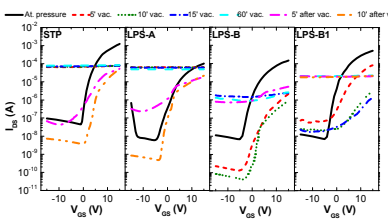
Fibril's influence



Extra anionic charge improves FET characteristics'

I_{DS}–V_{GS} transfer characteristics of the paper gated GIZO FETs at V_{DS} = 15 V.

Environmental stability



I_{DS}–V_{GS} transfer characteristics of the paper gated GIZO FETs at V_{DS} = 15 V obtained under vacuum and after recovery at atmospheric pressure.

- ✓ Field effect is lost under vacuum.
- ✓ More compact paper is less sensitive.
- ✓ Gate leakage also sensitive to environment.

- FETs' performance depend on the paper (fibers) used, gate leakage current in paper FETs can be reduced using a dense micro/nano fiber cellulose (M-NFC).
- M-NFC pulp modified by HCl addition improve the FETs characteristics':
  - μ_{sat} of the devices is improved up to 16 $cm^2 V^{-1} s^{-1}$, with an I_{on}/I_{off} ratio close to 10^5.
- FETs present susceptibility to the environment moisture (M-NFCs paper takes longer to establish equilibrium with environmental RH).

Summary

- Planar dual-gate oxide-based transistors were produced successfully on paper using it simultaneously as substrate and dielectric. The devices presented good electrical properties with I_{On}/I_{off} of 4 orders of magnitude and saturation mobility of ≈ 3 $cm^2.V^{-1}.s^{-1}$. When using this kind of configuration we are able to tune the on-voltage by almost 20 V depending on the applied voltage at the secondary gate (from +15 V to -15 V).
- The FETs performance depend of the V_{GS2} applied; easily the V_{on} can be modulated to the required voltage through secondary gate electrode. This particularity makes this devices attractive for logics or biosensors applications.
- The FETs produced on M-NFC paper exhibited a saturation mobility up to 16 $cm^2.V^{-1}.s^{-1}$ and an I_{On}/I_{Off} ratio close to 10^5, being simultaneously less sensitive to abrupt changes in the relative humidity than conventional pulp papers. The small fibrils (width in the nanoscale range) and their surface properties (compact and smooth) strongly bind water to M-NFC paper.
- Gate leakage current in paper FETs can be reduced using a dense micro/nano fiber cellulose (M-NFC).

UNINOVA i3N FCT FACULDADE DE CIÊNCIAS E TECNOLOGIA UNIVERSIDADE NOVA DE LISBOA